Land Pattern Design Guidelines for Fine Pitch Surface Mount Packages

Introduction

WJ Communications offers a wide variety of semiconductor products in plastic encapsulated, fine-pitch, surface-mount packages. These industry standard packages include, but are not limited to, SOT-89, micro-X SOT-86), SOIC-8, QFN, DFN, and SOT-363. The small footprint of these packages is attractive as it conserves valuable real estate on printed circuit boards (PCB's), simplifying part placement and the routing of traces. These devices may be either leaded, like the SOIC-8, or leadless, like the 6x6mm QFN's (Figure 1).

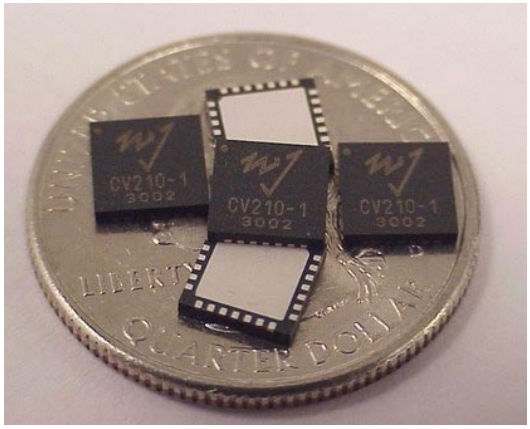

Figure 1: Examples of WJ devices in 6x6mm QFN packages

Some of the packages like the QFN's (Figure 1) have a ground paddle on the bottom of the device that must be soldered to the PCB. This paddle provides an excellent ground for the device, and offers a conduit through which heat can be transferred from the semiconductor die to the PCB and ultimately to a heat sink. Heat sinking is required in order to maintain the junction of the device at an acceptable temperature so that long life and reliable performance may be achieved.

Most designers are familiar with typical surface-mount requirements for devices that do not dissipate more than a few tenths of a Watt of dc power, and therefore do not need special care in heatsinking. However for devices that do dissipate at least this much dc power, special considerations are required in the design of the ground pad on the PCB. In order to ensure adequate heat transfer through the PCB, a pattern of vias is placed in the ground pad to connect the copper layer on the topside of the circuit board with copper layers within the board, and on the bottom of the board. This presence of vias in the ground pad requires that steps be taken to prevent solder from wicking through the vias, leaving voids under the device, and producing solder bumps on the opposite side of the board. These issues are addressed in this application note.

PCB Layout Guidelines

It should be noted the following information is intended only as a guideline and is general in nature. Many other factors must be taken into consideration during the PCB design phase: specific application, the end-user's own in-house layout / design rules, actual experience and development efforts for surface mount devices. Additionally, the end-user's PCB assembly house should have their own guidelines established for their particular capabilities. Together, these factors will ultimately define the final PCB layout and processes for successful mounting of the fine pitch, surface mount device.

Solder Mask Design / Considerations

Two types of land patterns are used in defining the solder pads for surface mount devices:

1. Solder Mask Defined (SMD) – Solder mask openings smaller than the mounting pads (Figure 2).

2. Non-Solder Mask Defined (NSMD) – Solder mask openings larger than the mounting pads (see Figure 2).

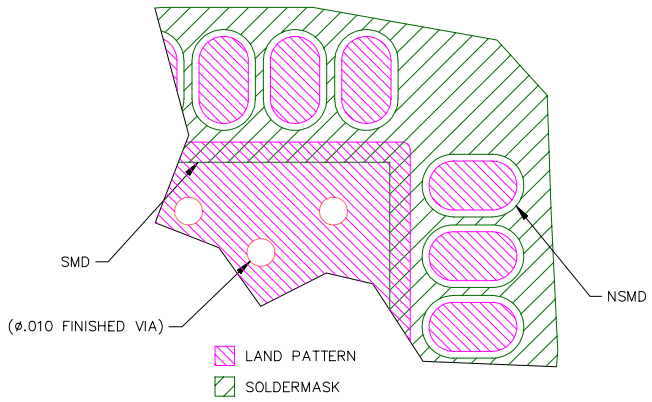

Figure 2: Example of SMD and NSMD Land Patterns

Better control of the copper etching process as compared to the solder masking process makes NSMD preferable. Using NSMD improves the reliability of solder joints as solder is allowed to "wrap around" the sides of the metal pads on the PCB[1].

The solder mask opening should be 120 to 150 microns (5 to 6 mils) larger than the pad size resulting in a 60 to 75 micron (2.5 to 3 mil) clearance between the copper pad and solder mask on all sides. This allows for solder mask registration tolerances, which are typically 50 to 65 microns (2 to 2.5 mils), depending upon the board fabricator's capabilities. To preclude solder

"bridging," typically each pad on the PCB should have its own solder mask opening with a web of solder mask between two adjacent pads. A web of solder mask should also be present between the pads and ground paddle. This web, along with the pad geometry will result in the necessary solder filleting required for a reliable solder joint. For leadless packages, it should be noted that although the ends of the pins are not plated; the plating usually smears on the ends during the package singulation process and it is expected that toe fillets may be formed. This is similar to gull winged QFN type packages where the fillets are formed on the end even though the ends are not plated[2]. A similar phenomenon occurs during the singulation of leaded packages, resulting in a fillet on both the heel and the toe side of the leads.

As an example, WJ Communication's 6x6 mm QFN package utilizes a 4.20mm square backside thermal / ground paddle with 0.65mm pitch leads. The associated PCB mounting pad is also 4.20mm square. In order to maximize the solder mask barrier between the leads and the large pool of solder on the ground pad, the solder mask around the ground pad has no gap around its perimeter. In spite of the lack of gap, the ground paddle and leads are all NSMD (Figure 3).

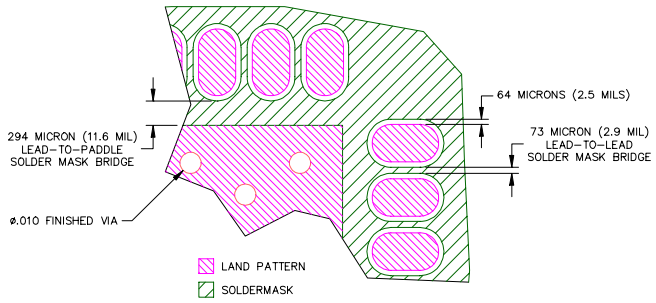

Figure 3: Illustration of Pad/ Solder Mask Clearance and Solder Mask Bridge

Thermal Via Design

In order to effectively transfer heat from the top metal layer of the PCB to the backside of the board and to the heatsink, thermal vias need to be incorporated into the thermal pad design. Care should be exercised when designing the thermal vias. If the vias are too large after plating, solder will be pulled away from the thermal pad (solder wicking) during the reflow process, resulting in undesirable and possibly detrimental voids. To minimize wicking, a 0.25mm (0.010 in) diameter finished via is recommended. If a 0.34mm (0.0135 in) diameter hole is drilled and plated with 1-ounce copper, it yields a 0.25mm (0.010 in) diameter finished via.

Even with small vias, some wicking will inevitably occur. Surface mount assembly houses employ a variety of practical methods to minimize solder wicking and uncontrolled flow of solder to the backside thermal land pad. Following is a brief list of those methods:

1) Apply polyimide (Kapton®) tape to the backside of the PCB opposite the device (Figure 4). During reflow, solder fills the vias and the tape prevents solder from flowing over the backside thermal land pad (Figure 5). Additionally, this method keeps the thermal contact area flat – crucial if a heatsink is employed.

   WJ Communications uses this particular method in the assembly of application boards for devices with ground pads.

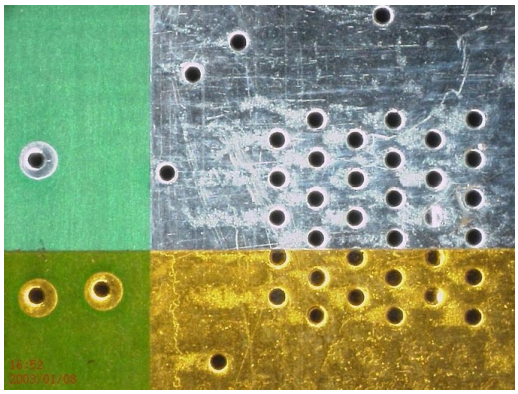

Figure 4: Example of Kapton® Tape On Thermal / Ground Pad

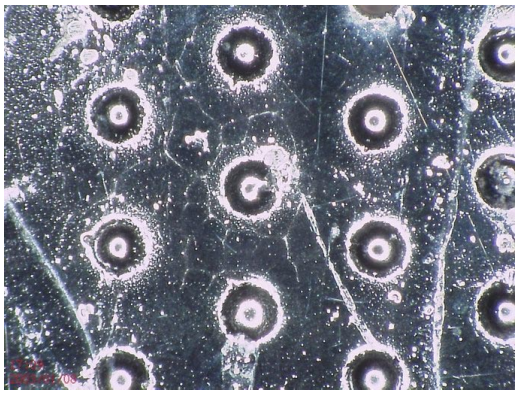

Figure 5: Solder-Filled Vias After Kapton® Tape Removal

2) Employ a no-shrink via filler material (e.g. Peters SD 2361) which is typically screen printed into the vias and then cured. The no-shrink is an important feature in that the shrinkage will allow fluxes and other materials to seep along the plug leading to electrical failures and electromigration.

3) Apply a solder mask "dam" to prevent excess solder flow on the backside of the PCB (Figure 6). During reflow, solder fills the vias, but spreading on the backside thermal land pad will be limited by the solder mask dams. Note

that the exposed thermal / ground pad is equal in area to that covered by the solder mask (see Figure 7). It should be noted this method is not conducive to heatsink mounting, as the wicked solder will create small "bumps" preventing good thermal contact.

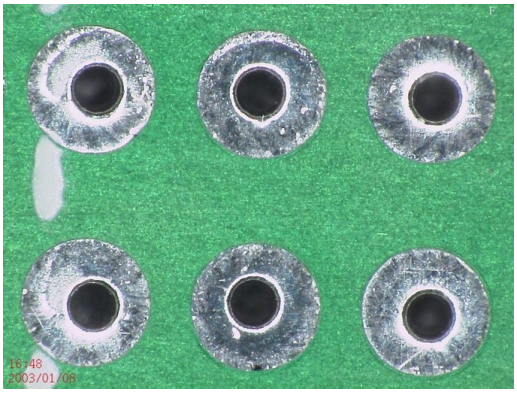

Figure 6: Example of Solder Mask "Dam"

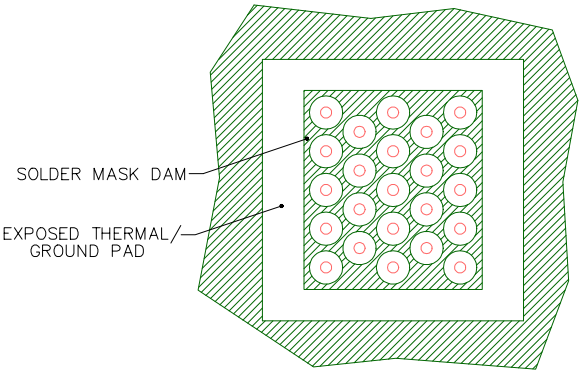

Figure 7: Exposed Thermal/Ground Pad

4) Tenting is a method whereby the vias are plugged with solder mask, either from the top or bottom surface of the PCB. Tenting from the top is considered the better option as it results in smaller voids under the ground pad. Solder masking of vias from the bottom side can result in increased outgassing during reflow and creating bigger voids around vias. It should be noted that WJ Communications has no device performance data on the effect of topside solder mask.

Cautionary Note: Manual Attach of SMT Devices to a PCB

Devices of the type described in this application guide are designed for automated SMT only. If necessary, manual attachment to a PCB requires careful consideration. Minimal, localized heat should be used to accomplish the attachment of the device or rework of nearby components. Failure to adhere to this guideline could result in delamination and failure of the device. Further details and suggestions for manual soldering of QFN packages are given in the application note, "AH201/QFN Package Hand-Soldering Application Note."

Summary

WJ Communications offers a wide variety of products in fine-pitch, plastic encapsulated packages that have a small footprint, which conserves valuable PCB real estate. Some of these devices utilize a ground pad to provide excellent electrical and thermal performance. Several points must be considered when designing the land pattern for these devices on a PCB:

- On devices with a ground pad, thermal vias connected to inner and backside copper layers are essential for providing proper heatsinking of the device.
- Maintain solder mask at the lead-to-lead and lead-to-thermal / ground pad interfaces to prevent solder bridging during reflow soldering.
- Uncontrolled wicking of solder through the thermal vias should be avoided. Surface mount assembly houses employ a variety of methods to control solder flow.
- Final PCB design is dependent upon a number of factors including the end user's particular application, and PCB assembly house guidelines for surface mount devices.

References

1. Intersil Technical Brief TB389.1: "PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages", October 2002.
2. Amkor Technology: "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages", March 2001.

Additional Application Notes

(located on WJ website at http://www.wj.com. The following bullets are also hyperlinked)

- AH201/QFN Package Hand-Soldering Application Note
- AH201 Mounting Considerations for Medium Power Surface Mount RF Devices
- CVxxx Series - Device Junction Temperatures vs PCB Mounting Configuration